

SYSTEM AND METHOD FOR ASSURED BUILT IN SELF REPAIR OF MEMORIES

ABSTRACT OF THE DISCLOSURE

5 An embedded memory device having improved BISR capabilities is provided.

 The embedded memory device includes an internal clock signal for use in accessing a
memory array having access to redundant memory cells during normal operation, and a
stress clock signal, wherein each pulse of the stress clock signal is of a shorter duration
than each pulse of the internal clock signal. Further included are a built-in self-test circuit
10 that performs a built-in self-test using the stress clock signal, and a register that stores
defective memory addresses detected by the built-in self-test circuit. Redundant control
logic is also included that redirects memory access operations to the defective memory
addresses to redundant memory cells.